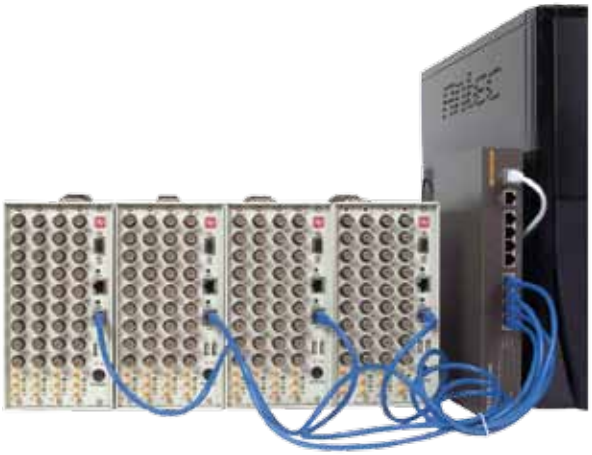
Data Physics Corporation

ABACUS™



The Abacus is a high performing, scalable realtime analysis engine for dynamic signal analysis. Each Abacus can be configured from 4-32 input channels, and each system can be connected for a virtually unlimited channel count. The scalable channel configuration and the variety of measurements available make the Abacus hardware a powerful and flexible tool for the test engineer.

DYNAMIC RANGE REALIZED

While there are many instruments that use 24 bit ADC chips, the Abacus was the first to incorporate analog components of the higher sampling dynamic range. The result is a consistent set of higher specifications for all measures of performance. When you look closely at specifications for Dynamic Range, Signal to Noise Ratio, Total Harmonic Distortion, Alias Rejection and Channel to Channel Phase Match, you can see the Abacus is a front end that does justice to the 24 bit digitizers.

The Abacus was the first system able to deliver 150 dB dynamic range in a spectrum, the entire potential of the 24 bit ADC. At its full bandwidth, the dynamic range is 120 dB, a testament to the analog design and the 24 bit Delta Sigma technology. At smaller bandwidths the dynamic range increases, reaching 150 dB at bandwidths below 1000 Hz.

POWERFUL AND SCALABE WITHOUT LOSS OF PERFORMANCE

A single Abacus is a portable instrument that connects to the host computer via Ethernet. The chassis can contain up to 32 inputs, 8 outputs, and 8 dedicated tachometer inputs. The input and output channels use 24 bit ADCs and DACs. The Abacus also uses an on-board Pentium processor to supervise traffic and support streaming data to local disk.

When more than 32 input channels are required, multiple Abacus chassis are connected to the host. Ethernet provides a convenient solution to the connectively and synchronization problems. To enable all channels in the multiple chassis to be simultaneously sampled, a clock signal is distributed via synchronizing cable. By using the same technology as Ethernet, the synch cable is able to distribute the sampling clock at speed up to 200 kHz from chassis to chassis. The synch cables come in calibrated lengths up to a maximum of 31 meters (101 ft.), and a delay compensation circuit in each Abacus chassis applies the precise delay to align the samples within the specifications for channel to channel matching.

REALTIME MEASUREMENTS ON ALL CHANNELS WHILE RECORDING TO DISK AT FULL BANDWIDTH

Each Abacus input channel contains its own ADC, and each Abacus module contains its own signal processor. This DSPcentric design is essential to the high realtime analysis bandwidth

of the system. Even when performing decimation filtering, the 1 Gigabit DSP has plenty of spare capacity to always maintain realtime measurements.

Each Abacus chassis contains its own disk storage. The local bus disk is essential to the high realtime recording rate of the system. Data can be stored locally on each system at an aggregate rate of 20 Mbytes/sec. **Whether using a mere eight channels in a single chassis or over a thousand channels distributed over 32 chassis, the system retains the same high specifications and throughput capacity.**

HARDWARE SPECIFICATIONS

INPUT

4 to 32 per chassis
ADC Resolution (Analog AAF): 24-bit
Sample Resolution (Digital AAF): 32-bit floating point
Coupling: AC/DC, DIFF/SE, ICP, TEDS
Anti-alias Filters: 110 dB protection, all ranges
Dynamic Range: 120 dB to 150 dB
Input Ranges: 1/2/5/10 V full scale (25 V optional)
Input Impedace: 1 MOhm to GND, 50 SE shield to GND
Max Input Voltage: 80 vPeak, 2.5 vRmsShield(SE)
CMRR: 60 dB (typical), f < 40 kHz
Amplitude Accuracy:
  +/- 0.020 dB (0.2% FS) at 1 kHz for 15 degC < T < 40 degC
Amplitude Ripple: (Digital AAF) - 0.001 dB for 0< f < fS / 2.56
Amplitude Droop:
  (Analog AAF) - 0.005 dB at 5 kHz;
  0.010 dB at 25 kHz;
  0.050 dB at 49 kHz
Residual Offset: +/- 0.1% FS AND not larger than 3 mvDC
Phase Accuracy: 0.05 deg to 0.5 deg for DC to 40 kHz
Crosstalk between Inputs: < -100 dB
Crosstalk between inputs and source: < -90 dB
Input noise:
  1 V range: 20 nV/Hz, 3 µVrms @ 20 kHz BW
  10 V range: 160 nV/Hz, 24 µVrms @ 20 kHz BW
THD: 100 dB
Overload Detection: Both pre-filter and post-filter
Minimum SampleRate: less than 1 Sps
Maximum SampleRate: 107.42 kSps (214.82 kSps optional)
Sample rates: 83 steps, down to 1 Hz
Maximum useful Frequency: 49 kHz standard (97 kHz optional)
Frequency Accuracy: 25 ppm
Time Accuracy: 25 ppm

TACHOMETER INPUT

2 to 8 per chassis
Pulses Per Revolution (PPR): 0.01-4096
Pulses per minute: 1-300,000
Input Range: +/- 24 V FS
Adjustable threshold, hysteresis, holdoff, prescaling

OUTPUT

2 to 8 per chassis
Dynamic Range: > 120 dB
Resolution: 24-bit
Voltage range: 0.1/0.2/0.5/1/2/3/10 V Full Scale
Output Current: 10 mA Max; continuous short
THD: -100 dB (typical), -90 dB Max, f < 40 kHz
Reconstruction Filter: 100 dB image rejection
Output Waveforms: 65536 max blocksize for arbitrary; unlimited for recorded (optional)

NETWORK PERIPHERAL CHASSIS

Disk Capacity: 250 GB (320 GB optional removable drive)
Disk Rate: 20 MB/s streaming (32 + 8 channels 32-bit floating point samples @ 107.42 kSps)
Dimensions: 4 x 10 x 18 in. without trims
Weight: 20 pounds
Operating Temperature: 0 to 55° C
Power: 130 Watts

NETWORK TOPOLOGY

100 Mbps Ethernet chassis,
100/1000 Mbps Ethernet to host
Sampling: Common clock across chassis for synchronous sampling

NOTE: All specs hold both within and across chassis. Continued product improvement necessitates that Data Physics reserve the right to modify these specifications without notice.

Data Physics corporation

Discover more at www.dataphysics.com

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